Q5 Host Interfaces

Application Note

80548NT11882A Rev. 0 – 2021-03-22

Telit Technical Documentation

APPLICABILITY TABLE

PRODUCTS
SE868-V3
SE873
SE873Q5
SL876Q5-A

CONTENTS

1. INTRODUCTION

1.1. Scope

This document provides an overview of communication interfaces applicable to all GNSS module variants listed in the APPLICABILITY TABLE.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to develop their applications using the Telit GNSS modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report of documentation errors contact Telit Technical Support at:

- *TS-EMEA@telit.com*
- *TS-AMERICAS@telit.com*
- *TS-APAC@telit.com*
- *TS-SRD@telit.com*
- *TS-ONEEDGE@telit.com*

Alternatively, use:

https://www.telit.com/contact-us

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

https://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates the user feedback on our information.

1.4. Symbol Conventions

	**Danger:** This information MUST be followed or catastrophic equipment failure or personal injury may occur.
	**Warning:** Alerts the user on important steps about the module integration.
	**Note/Tip:** Provides advice and suggestions that may be useful when integrating the module.
	**Electro-static Discharge:** Notifies the user to take proper grounding precautions before handling the product.

Table 1-1: Symbol Conventions

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1.5. Related Documents

- Telit SE868 Hardware User Guide, 1VV0300964
- SE873_Product User Guide, 1VV0301216
- SL876Q5-A Product User Guide, 1VV0301333

2. OVERVIEW

This document describes the operation of the serial interfaces available in the GNSS modules listed in the APPLICABILITY TABLE.

At start-up, the Host port can be configured for one of the following three types of communications interfaces:

- UART
- I2C
- SPI

This is done by sensing the state of 2 pins at startup.

The serial port outputs are 1.8V logic levels, while the inputs are 1.8V to 3.6V tolerant.

2.1. Message Protocols

Two message protocols supported are:

- NMEA
- OSP (One Socket Protocol – Proprietary CSR / SiRF protocol)

The system does not support concurrent operation of NMEA and OSP protocols on the same serial port.

Either of these protocols can be used with any of the three communications interfaces (UART, I2C, or SPI).

Note/Tip: For further information about OSP protocol please contact Telit technical support.

3. HOST PORT IMPLEMENTATION

The devices listed in the APPLICABILITY TABLE support the following three types of serial interface for the host port:

- UART
- Multi-master I2C
- Slave SPI

3.1. Configuration Settings

An internal RESET occurs when either:

- Power is first applied to the device;
- The external NRESET input is asserted and released

The corresponding pinout for the devices is:

- SE868: NRESET (pin 12)
- SE873/SE873Q5: NRESET (pin 8) (reset in electric diagram)
- SL876Q5-A: NRESET (pin 1)

The Host Port Select pins are read upon either of the following conditions:

- An external RESET occurs.
- The first time ON_OFF is asserted after an internal reset

See section 3.1.1 Host Port Type Selection for usage of these configuration pins.

Note/Tip: When connected to a host or other interface device, the product designer must assess and control the risk of any external drive or inadvertent leakage into these lines to ensure that the correct configuration is selected.

3.1.1. Host Port Type Selection

The following table indicates the required state of the host port type selection pins during the startup sequence to select the desired communication mode.

SE868-V3 pin	SE873/Q5 pin	SL876Q5-A pin	Pullup/ Pulldown	UART	I2C (multi-master)	SPI (slave)
23 GPIO 6	13 GPIO 6	16 GPIO 6	weak internal pulldown	Pullup (10 kΩ to +1.8 V)	Float	Float (becomes SPI CLK)
24 GPIO 7	12 GPIO 7	6 GPIO 7	Weak internal pullup	Float	Pulldown (10 kΩ to ground)	Float (becomes SPI_CS)

Table 3-1: Host Port Type Selection

For the SPI setting, you must ensure that both GPIO 6 and GPIO 7 remain float. Therefore, SPI_CLK and SPI_CS signals must be connected only after the startup phase.

3.2. Host Port Pin Identification and Logic Levels

3.2.1. Host Port Pin Identification

The following table indicates the signals for the host port pins after host port selection is done.

SE868-V3 Pin	SE873/Q5 Pin	SL876Q5-A Pin	Interface Signal Names		
			UART	I2C	SPI (slave)
10 : TX	15 : TX	17: TX	TX	SCL (I2C_CLK)[3]	SSPI_DO MISO
11 : RX	14 : RX	15 : RX	RX	SDA (I2C_DATA)[3]	SSPI_DI MOSI
23 : GPIO6[1]	13 : GPIO 6[1]	16 : GPIO 6[1]	Not Used or may be CTS[2]	Not Used	SSPI_CLK (SPI slave clock input)
24 : GPIO7	12 : GPIO 7	6 : GPIO 7	Not Used or may be RTS[2]	Not Used	SSPI_CS (SPI select – active low)
GPIO 4	GPIO 4	GPIO 4	DRI	DRI4	DRI

Note 1: GPIO6 and GPIO7 may require pullups or pulldowns during startup to select the port type. See Table 3-2: Host Port Pin Identification
Note 2: see Section 4.1 UART Flow Control
Note 3: the I2C protocol requires pullups on SCL and SDA. See Section 5.1.1 I2C Electrical
Note 4: DRI is available only in slave mode, not in multi-master mode.

Table 3-2: Host Port Pin Identification

3.2.2. Host Port Logic Levels

Serial outputs are CMOS 1.8V levels and may require an external level shifter to interface with a 3.3 V Host input.

Input pins are 3.3 V compatible. However, if serial Input is driven from a source higher than 1.8 V, excess leakage current may flow through the ~80 kΩ internal pull-up resistor

3.3. Data Ready Indicator Pin

Note/Tip: This pin is not functional unless a correct Firmware version is installed. Contact Telit support for details for using this signal.

You can use GPIO4 as a message-ready indicator to simplify the host interfacing. If there is no data to transmit, GPIO4 stays low. GPIO4 goes high when data is ready to be sent out and after completion of all data transmission, it goes low again.

Note/Tip: DRI does not work in I2C multimaster. All other modes are supported.

3.4. Data Rates and Timing Considerations

3.4.1. Input

The serial port is ready after the baseband has been started with an ON_OFF pulse, at which time an OK to SEND message (NMEA message $PSRF150,1 or OSP Message ID 18) is transmitted.

Input commands are generally processed within 100 ms of receipt.

Commands can be sent continuously but at least one second must be allowed for their processing.

The maximum sustained command input is about 10,000 characters per second. Therefore, the full bandwidth should not be utilized at rates above 115.2 kbps. Command processing is a low priority task within the system.

The minimum recommended baud rate for OSP is 38400, or 115200 if debug data messages are enabled.

The module can support serial port operation at speeds above 115.2 kbps for data download of EE files and loading flash memory.

Low data rates impact startup and TTFF times in sending configuration commands, EE data.

For example, downloading a single EE data block for one satellite in NMEA at 4.8 kbps will take about ½ second. Refer to EE documentation for the sizes of various messages and files.

3.4.2. Output

Selection and rate of delivery of some output messages can be configured via OSP or NMEA commands.

Debug messages are controlled as a block and cannot be individually selected.

Messages associated with a request and transfer of EE data between the host and the module may not be configurable.

Some event or alarm messages occur spontaneously and cannot be directly controlled.

The designer must assess the capacity of the communications link between the module and the host. Select OSP or NMEA messages appropriate to the application and well within the maximum capacity of the communications link. In assessing the capacity required, consider the protocol overheads and maximum size of variable payloads.

In applications where power consumption is critical, time spent creating and sending messages causes both the module and the host to consume power. A low data link speed increases the current consumption during data transmission.

When switching the unit to hibernate mode controlling shutdown with ON_OFF signal or by OSP/NMEA command message, the module will continue to run until the transmit/output buffers are emptied.

At slow serial port speeds with a high volume of data, time-to-turn-off may be up to one second. If host flow control prevents output of final messages, the module will not turn off.

4. UART

UART is commonly used for GPS data reporting and receiver control.

UART features include:

- Transmit and receive channels contain FIFO buffers
- Serial data rates are selectable from 4.8 kbps to 1.2288 Mbps.

Warning: Baud rate higher than 115.2 kbps should not be used.

4.1. UART Flow Control

4.1.1. No Hardware Flow Control

- Only RX and TX data lines are used.
- No hardware or software flow control is available.

4.1.2. Hardware Flow Control

Note/Tip: This configuration is not available in all firmware versions.

Hardware flow control may be configured via an OSP command.

- RX and TX lines are used for data transmission.
- RTS and CTS for hardware flow control are available:
    - When CTS is low, transmission stops at the end of the current character. It restarts when CTS goes high.

Note/Tip: Note that module may lose or garble serial messages if host flow control throttling is too severe. System design assumes unrestricted outflow of serial messages.

4.2. UART Operation

4.2.1. UART TX/RX Electrical

- "1" (mark) is logic high
- "0" (space) is logic low
- Idle line is logic high
- Line-break/open line is continuous logic low. (Continuous break is not allowed on RX during operation and not generated on TX during operation.)

4.2.2. UART Frame Format

- 1 start bit
- 8 data bits (only) with least significant bit (bit 0) to most significant bit (bit 7)
- 1 stop bit followed by either the next character or an idle line
- Parity is not used

Designers should treat computations of maximum message output capacity based on 11-bits per character. This effectively decreases line capacity by about 10% and increases CPU and host ON time for message exchange by about 10%.

4.2.3. UART Data Rates

4.2.3.1. UART Default Data Rate

At boot up, the default data rate depends on the protocol selected:

- OSP: 115200 baud
- NMEA: 9600 baud

Software can set the rate depending on the type of operation, such as FLASH code upload.

4.2.3.2. UART Selectable Data Rates

- Not all possible data rates are supported by every firmware version.
- UART data rates are: 4.8, 9.6, 19.2, 38.4, 57.6, 115.2, 230.4, 460.8, 921.6 and 1228.8 kbps.
- Higher data rates can be configured but have not been tested.

Note/Tip: Operation at rates above 115.2 kbps have not been rigorously tested and verified.

- Because UART transmission is asynchronous and sampled by the receiver, both sender and receiver require closely matched bit-rate clocks.
- Data bit waveform and timing distortion must be limited.
- Maximum allowed clock rate difference between the module and the host is 2.0% overall.
- Maximum bit-edge distortion is 5% UI and maximum bit jitter is 5% UI.
- Unit Interval (UI) = (1 / data bit rate)

5. I2C

The modules support two-wire I2C operation.

For more information on I2C interfaces and operation, refer to industry documents.

5.1. I2C Description

5.1.1. I2C Electrical

All device drivers are specified as open drain with external pull-up to allow collision detection and contention resolution.

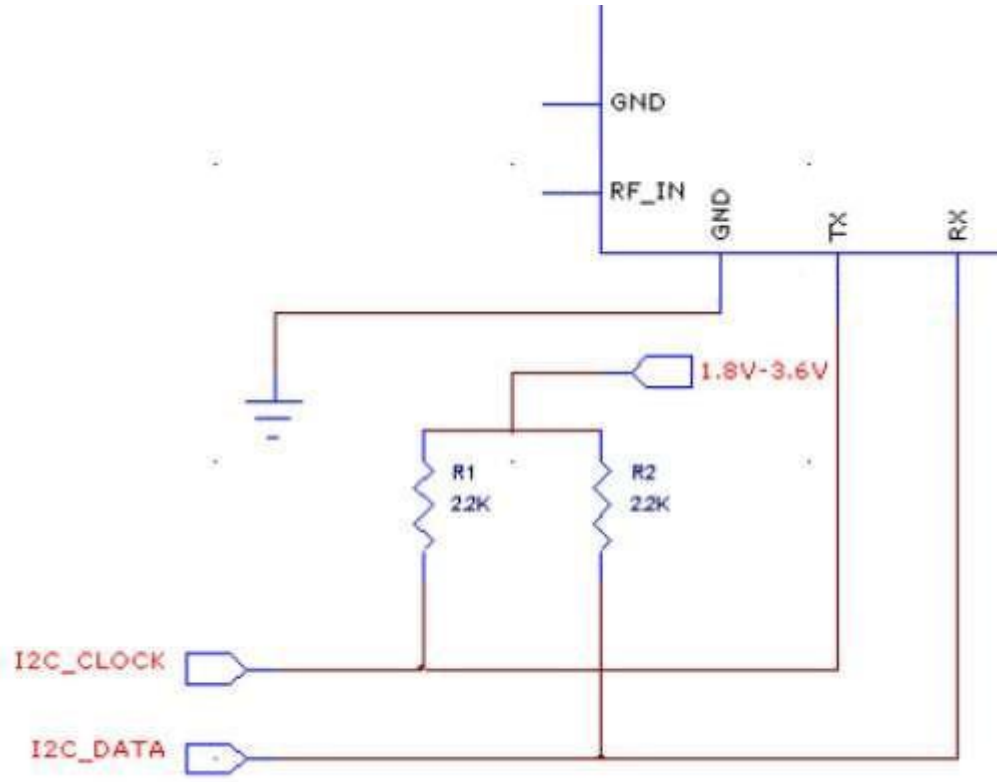


Figure 5-1: I2C Required Pullups

Note/Tip: For proper operation, external pull-ups are required to ensure proper rise times with stray shunt capacitances from attached loads and traces. These must be pulled up to 1.8V-3.6V supply. The typical resistor value is between 1KΩ and 2.2KΩ.

5.1.2. I2C Frame Format

I2C-standard 8-bit octets (bytes) are used. Bit order is MSB transmitted first, with the first byte of a transfer containing the 7-bit address and direction bit per the standard. The direction bit is set to '0' indicating write or send in all transfers involving the module. There is no specified maximum limit of bytes per transfer.

5.1.3. I2C Supported Modes

The supported modes are:

- Multi-master
- Slave

The multi-master mode has a behavior similar to UART operation.

Note/Tip: The module cannot switch between the supported modes at runtime. Each mode requires a specific firmware configured accordingly. For more information about modes, please ask Telit technical support.

5.1.4. I2C Multi-Master Mode Considerations

Note that the module may lose or garble serial messages if contention with other bus masters makes it unable to send all messages. System design assumes unrestricted outflow of serial messages.

When switching the module to hibernate mode using orderly shutdown with ON_OFF pulse or by OSP/NMEA command message, it will continue to run until the I2C transmit buffers are emptied.

At slow I2C serial port speeds with a high volume of data, time-to-turn-off may be up to one second with no throttling from contention.

If multi-master mode contention on the I2C bus prevents output, the module will take longer to turn off. If the I2C bus is inadvertently seized (another device hold clocks or data line low and never releases) the module will not turn off.

When there are more than two devices on the I2C bus, they must be all multi-master. If there are only two devices (one receiver and another one), if the receiver is multi-muter, the other can be slave.

5.2. I2C Operations

5.2.1. I2C Data Rates

The supported bit clock rates are 100 kbps (standard mode) and 400 kbps (DEFAULT - fast mode). High speed mode is not supported. The data rate can be changed using an OSP command (MID 178, SID 71).

The maximum I2C data handling capacity between sender and receiver must be de-rated by protocol overheads, collision density, and backoff/retry timing.

5.2.2. I2C Addresses

Address format is 7-bit. I2C supports multiple masters and multiple slaves.

When the module is the master, it addresses the host CPU at the address 0x62.

When the host is master, the module responds to address 0x60.

The module's I2C master and slave addresses can be changed under firmware control using OSP command (MID 178, SID 71).

5.2.3. I2C Message Transfer

5.2.3.1. Multi-Master Mode

Multi-master mode requires that the hardware detects and arbitrates between collisions for master status and data direction. Master or slave mode is determined from clock contention: whichever device is generating the clock is master, and all other devices on the bus are slave. In the event of contention time-out, the master device must take control of error detection and retries. If a device has data to send, it waits for the bus to idle, then asserts itself as master and sends the data.

Thus, in a typical application, the module periodically asserts itself as bus master and sends messages to the host. If the host wants to send a command to the module, it must assert itself as master when the I2C bus becomes idle, and then send the command. If the module has a response to the command, it becomes the master again and sends the reply.

If both the module and the host try to assert bus mastership simultaneously, the module executes the contention resolution mechanism specified by the I2C standard.

5.2.3.2. Slave Mode

Slave mode requires a master device connected to the bus which generates the clock.

5.1. I2C Details

The following internal operation details are provided for information only:

- Internal FIFOs for RX and TX are provided.
- Bus contention timeout is set to 30 ms and is not changeable.

6. SPI

Firmware currently supports only the SPI format, not MicroWire. The module operates only as SPI slave. This requires that the host drive the SPI clock and SPI chip select lines when it wishes to receive messages from the module. The maximum clock frequency supported is 6.8MHz. Daisy chain or "cascaded" clock mode is not supported. Frame size is 8 bits, with MSB sent first. There are no unique SPI headers; the payload is the same structure as the message. NMEA messages and OSP messages each have their own unique start-of-message, end-of message patterns and message data structures. All channel recovery, message sequencing, and integrity checks are the responsibility of the SPI master.

Note/Tip: Because of the unsupported daisy chain mode, only one slave device can be connected to the bus.

6.1. SPI Description

Figure 6-1: SPI Master-Slave Connection

The four SPI pins are:

- SPI Data Input (Master Out, Slave In - MOSI)
- SPI Data Output (Master In, Slave Out - MISO)
- SPI Select Input (CS)
- SPI Clock Input (SCK)

6.1.1. SPI Clock Polarity and Phase

There are four modes of communication between the master and slave depending on the clock polarity and clock phase with respect to data.

CPOL defines the polarity of clock and CPHA defines the clock phase.

When CPOL is zero, the clock stays low and the status of clock phase is determined by CPHA.

- If CPHA is zero, data is read on the clock's rising edge and changed on a falling edge.
- If CPHA is high, data is read on the clock's falling edge and changed on a rising edge.

When CPOL is one, it is opposite of when the CPOL is zero. The clock stays high in the idle state.

- If CPHA is zero, data is read on clock's falling edge and data is changed on a rising edge.
- If CPHA is one, data is read on clock's rising edge and data is changed on a falling edge.

It is important that the CPOL and CPHA match between the master and slave. These are set in the module by default to CPOL = 0, CPHA = 1, and cannot be changed under normal circumstances. The combinations of polarity and phase are often referred to as modes, which are commonly numbered according to the following convention:

Mode	CPOL	CPHA	Comments
0	0	0	Not Supported
1	0	1	Supported
2	1	0	Not Supported
3	1	1	Supported (requires custom software)

Table 6-1: SPI Modes of Operation

Please note that only two modes out of four are supported, and to change from default mode 1 to mode 3 special software is required from Telit.

6.1.2. SPI Considerations

When the serial interface is configured for SPI mode, the internal framing logic is powered up in the hibernate state. Accidental toggling of the SPI clock line while SSPI_CS is enabled will step the framing register requiring software logic on the host to recover frame synch.

When switching to the hibernate state using orderly shutdown (with an ON_OFF signal or by command), the module will continue to run until the SPI transmit/output buffers are emptied. At slow serial port speeds with a high volume of data, time-to-turn-off may be up to one second.

If the host stops polling or turns off the SPI clock before the TX FIFO is empty and idle patterns are sent to host, the module will never turn off.

6.1. SPI Operation

6.1.1. SPI Initialization

To communicate properly between SPI devices, the exact protocol must be agreed on, including the SPI mode and an idle byte pattern. The master can periodically transmit the idle pattern (A7B4) and poll the module for the same pattern. This indicates that the slave is ready to communicate but has nothing to transmit. After power up, the module will transmit the OK to SEND message after about 100 ms, indicating that the module is ready to receive.

6.1.2. SPI Message Transfer

To begin a communication, the master pulls the SPI Chip Select (SPI_CS) pin low and generates a clock frequency (less than or equal to the maximum frequency supported by the slave device). During clock generation, full duplex transmission occurs:

- The master sends data on its SDO (MOSI) line; the slave reads from its SDI line
- The slave sends data on its SDO (MISO) line; the master reads from its SDI line

Each device transmits Idle characters when it has no data to send.

The host (master) is expected to transmit the idle pattern when it is querying the module unless it has messages to transmit. This keeps processing overhead low since hardware does not place most idle pattern bytes in the RX FIFO.

Most messaging from the module can be serviced by polling. Since message creation times may have about 200 ms of jitter from second-to-second, the host must start polling before messages are expected from the module. Any delay in polling increases the latency between position fix calculation and position fix reception by the host.

The Data Ready Indicator pin may be used as “message waiting” to signal the host that the module has data to send, and polling should be started. This indicator is unaffected by idle byte pattern.

When transmitting, the module fills its FIFO with as many queued up messages as it can fit. The host is required to poll messages until idle pattern bytes are detected. The module then replenishes its TX-FIFO with subsequent pending messages (if any).

Note that module may lose or garble messages if host does not poll often enough to fetch all messages. System design assumes unrestricted outflow of serial messages.

6.2. SPI Internal Details

The following internal operation details are provided for information only:

- TX and RX each have independent 1024-byte FIFO buffers
- RX and TX have independent, software-specified two-byte idle patterns
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken
- FIFO buffers can generate an interrupt at any fill level
- SPI detects synchronization errors and can be reset by software.

6.3. SPI Example Communications

At startup, the module is in NMEA protocol. Expect the module to transmit an OK to SEND message with a value of "1" to the host when ready to communicate. The master is supplying the clock and can communicate bi-directionally. When there is nothing to send, idle bytes are sent out. Figure 6-2 Example Startup Dialog displays this conversation

```
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
8:57:34.675      [ch:1]Batch Shift Done. batch=500; count=500
8:57:34.691      [ch:1]Cheetah Write
8:57:34.691      [ch:1][len:500]        a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
8:57:34.706      [ch:1]Cheetah READ
8:57:34.706      [ch:1][len:500]        ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
8:57:34.706      [ch:1]Batch Shift Done. batch=500; count=500
8:57:34.722      [ch:1]Cheetah Write
8:57:34.737      [ch:1][len:500]        a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
8:57:34.769      [ch:1]Cheetah READ
8:57:34.769      [ch:1][len:500]        ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
8:57:34.784      [ch:1]Batch Shift Done. batch=500; count=500
8:57:34.784      [ch:1]Cheetah Write
8:57:34.800      [ch:1][len:500]        a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
8:57:34.831      [ch:1]Cheetah READ
8:57:34.831      [ch:1][len:500]        24 50 53 52 46 31 35 30 2c 31 2a 33 45 0d 0a b4 a7 b4 a7 b4 a7 b4 a
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
8:57:34.847      [ch:1]Batch Shift Done. batch=500; count=500
```

Figure 6-2: Example Startup Dialog

Notes:

- "a7 b4" is the Idle pattern (no data available to send)
- "00 00" or "ff ff" are the null data message

The highlighted portion in Figure 6-2: Example Startup Dialog is the NMEA **OK to SEND**.

The message format is shown in the table below.

	Example	Description
Message ID	$PSRF150	PSRF150 protocol header
OkToSend	1	1 = OK to send, 0 = not OK to send
Checksum	*3F	
<CR><LF>	1	End of message termination

Table 6-2: OK-to-Send Message

The Table 6-2: OK-to-Send Message is:

```
24 50 53 52 46 31 35 30 2C 31 2A 33 45 0D 0A
 $  P  S  R  F  1  5  0  ,  1  *  3  E cr lf
```

Another example is shown in Figure 6-3: Example NMEA Message.

```
8:57:35.862      [ch:1]Cheetah write
8:57:35.862      [ch:1][len:500]        a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
8:57:35.878      [ch:1]Chetah READ
8:57:35.878      [ch:1][len:500]        a7 24 47 50 47 47 41 2c 32 33 35 39 34 36 2e 30 33 35 2
a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4 a7 b4
```

Figure 6-3: Example NMEA Message

Part of the NMEA message is:

```
24 47 50 47 47 41 2C 32 33 35 39
 $  G  P  G  G  A  ,  2  3  5  9
```

7. I2C AND SPI COMMUNICATIONS TESTING

This section provides a method for independently testing the I2C and SPI communications in designs implementing Telit's modules. This simple process can be utilized in cases where the system's software may not be ready or fully functional.

Telit uses an AARDVARK SPI/I2C to USB converter, available from Total Phase www.totalphase.com, to communicate with the module's serial port using the SPI or I2C protocols.

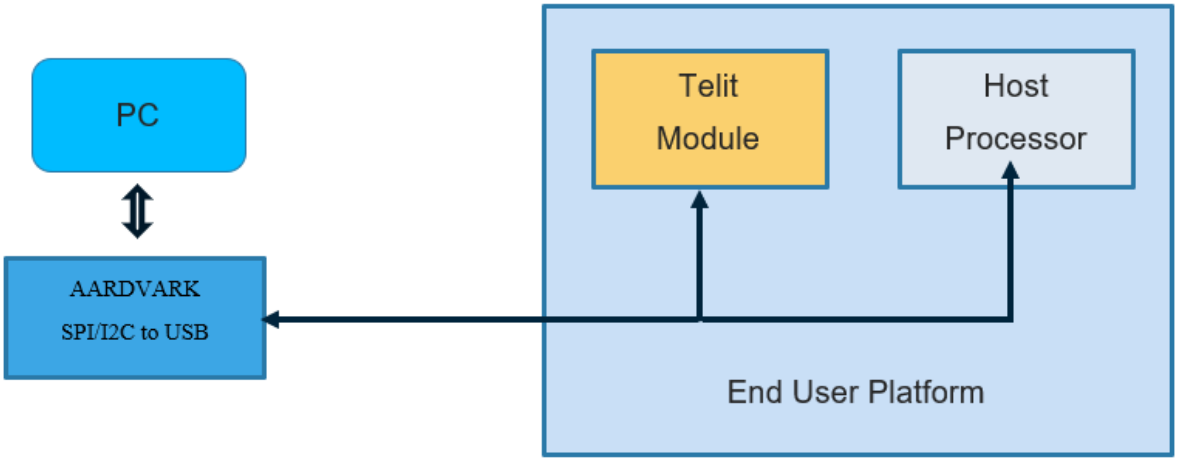


Figure 7-1: AARDVARK SPI/I2C to USB

Refer to Section 3.1.1 Host Port Type Selection for information about how to configure the port.

When the module is started, the serial port pins will be activated as shown in section 3.2.1 Host Port Pin Identification.

Before proceeding further, make sure the module is correctly powered, and out of RESET.

An ON pulse must be issued to bring the module out of hibernate mode. Allow at least 100 ms after the module is out of RESET, to issue the ON pulse. This must be a single pulse with least 10 ms duration.

Note: A second ON pulse will put the module back into hibernate.

The AARDVARK adapter comes with a CD which contains manuals, drivers, executables, and source code. *Please consult the AARDVARK manual for installation details.*

7.1. I2C

Follow the below steps to test the I2C:

1. Connect the module's I2C DIO and CLK to the corresponding pins on the AADVARD's ribbon cable.

1. Run the Aardvark GUI.exe program.
   This will open the Aardvark I2C/SPI Control Center.

2. Select the Configure Aardvark Adapter, as shown below.

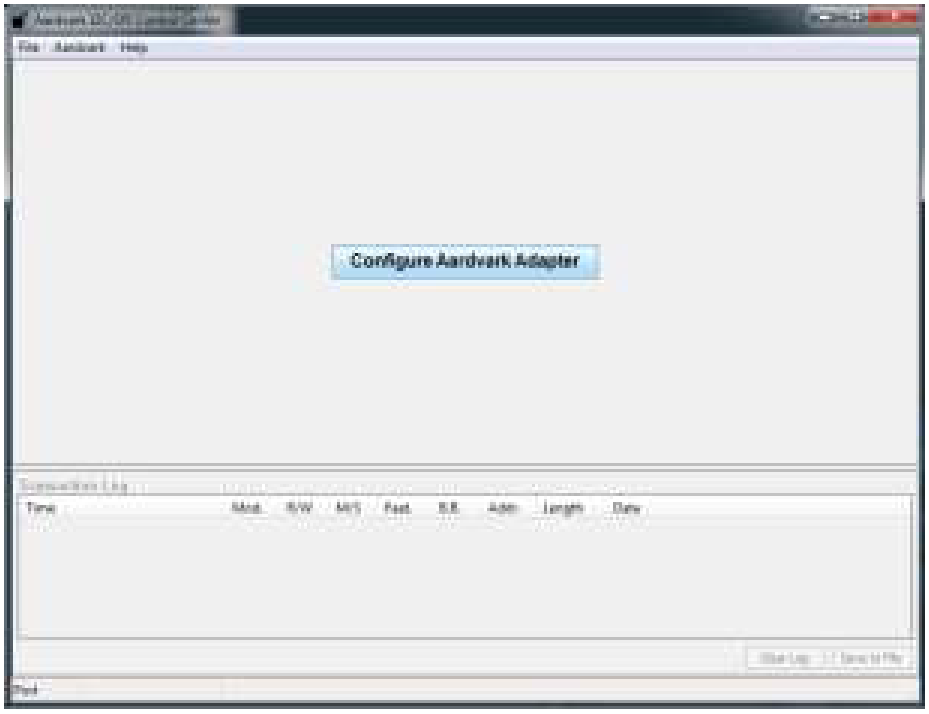


Figure 7-2: Configure Aardvark Adapter

3. Identify the Port where the Aardvark is connected and click **OK**.

Figure 7-3: Select an Aardvark Port

4. In the Aardvark I2C/SPI Control Center, set the Slave Addr to 0x60, and select the Master Read button.

---

1. **Note/Tip:** The master address is 0x62.

7.1.1. Slave Mode Test

If the transaction is successful, the Data column in the Transaction Log will display the data received from the module in hexadecimal.

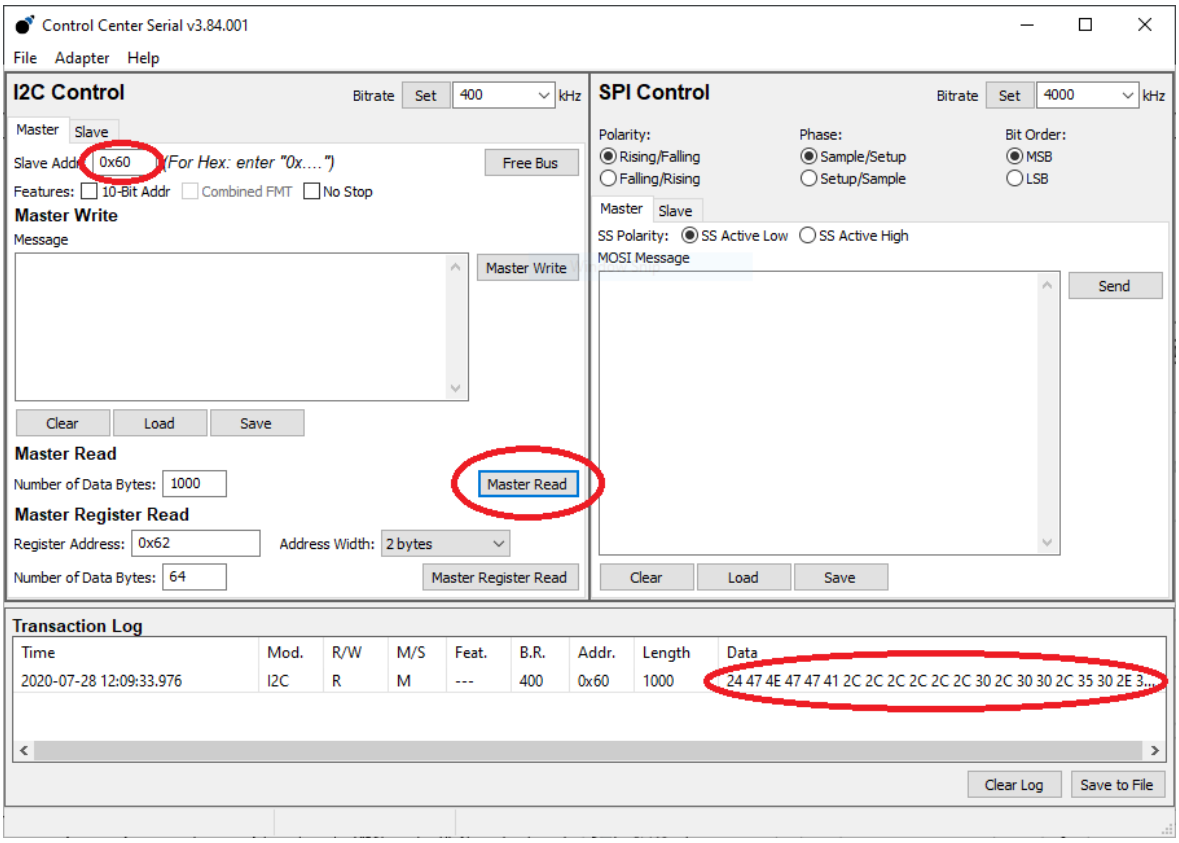
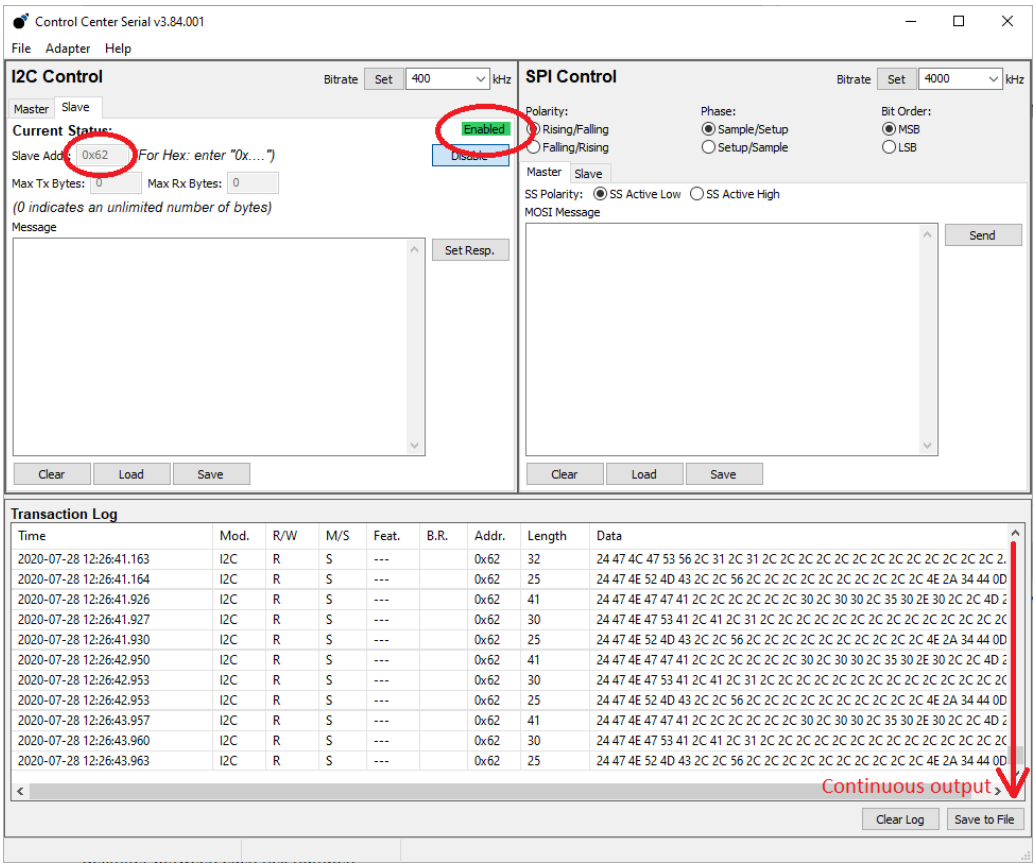


Figure 7-4: Successful I2C Communication Confirmation

This hexa decimal data confirms the successful I2C slave communications.

7.1.2. Multi-Master Mode Test



The continuous output confirms the successful I2C Multi-Master communications.

7.2. SPI

Follow the below steps to test the SPI:

1. Connect the module's SPI DO, DI, CS, and CLK to the corresponding pins on the AADVARD's ribbon cable.
2. Run the Aardvark GUI.exe program.
   This will open the Aardvark I2C/SPI Control Center.
3. Select the Configure Aardvark Adapter, as shown below.

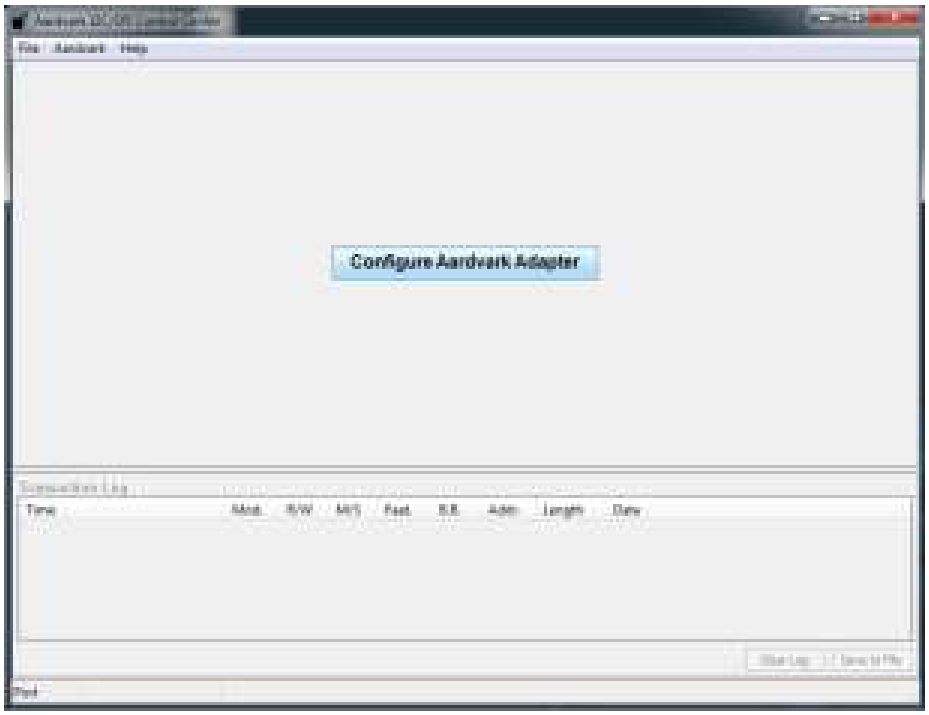


Figure 7-5: Configure Aardvark Adapter

4. Identify the Port where the Aardvark is connected and click **OK**.

Figure 7-6: Select an Aardvark Port

5. In the Aardvark I2C/SPI Control Center, select Setup/Sample for the Phase settings, to select SPI MODE1. This is the default mode for the Telit modules.

Note/Tip: Idle bytes must be sent to clock data out of the module's FIFO. The idle bytes format is 0xA7B4.

6. In the Aardvark I2C/SPI Control Center MOSI Message window, enter the idle bytes A7B4, and then click **Send**.

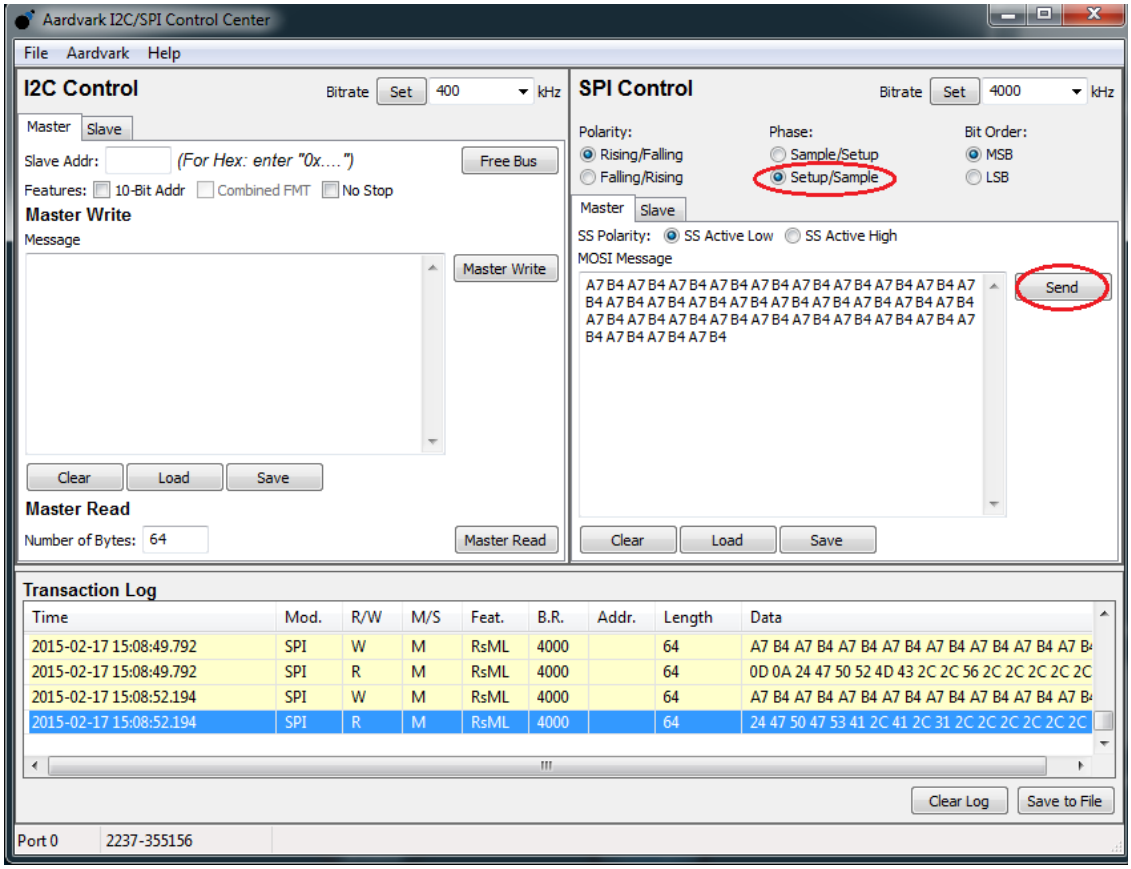


Figure 7-7: Aardvark I2C/SPI Control Center MOSI Message

If the transaction is successful, the Data column in the Transaction Log will display the data received from the Telit module in hexadecimal.

This confirms successful SPI communications with the module.

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- it can interfere with other electronic devices, particularly in environments such as hospitals, airports, aircrafts, etc.
- there is a risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product. Therefore, the external components of the module, as well as any project or installation issue, have to be handled with care. Any interference may cause the risk of disturbing the GSM network or external devices or having an impact on the security system. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed carefully in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The equipment is intended to be installed in a restricted area location.

The equipment must be supplied by an external specific limited power source in compliance with the standard EN 62368-1:2014.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

https://ec.europa.eu/growth/sectors/electrical-engineering_en

9. GLOSSARY

CLK	Clock
CMOS	Complementary Metal – Oxide Semiconductor
CPHA	Clock Phase
CPOL	Clock Polarity
CPU	Central Processing Unit
CS	Chip Select
CTS	Clear To Send
DI	Data Input
DO	Data Output
FIFO	First In First Out
GPIO	General Purpose Input Output
GPS	Global Positioning System
I²C	Inter-Integrated Circuit
I/O	Input Output
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
NMEA	National Marine Electronics Association
OSP	One Socket Protocol
RTS	Request To Send
RX	Receive
SDI	Serial Data Input
SDO	Serial Data Output
SPI	Serial Peripheral Interface
TTFF	Time To First Fix
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

10. DOCUMENT HISTORY

Revision	Date	Changes
0	2020-03-18	First issue

From Mod.0809 rev.2

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